Welcome to the World of Micro Electronics using Micron Interconnect

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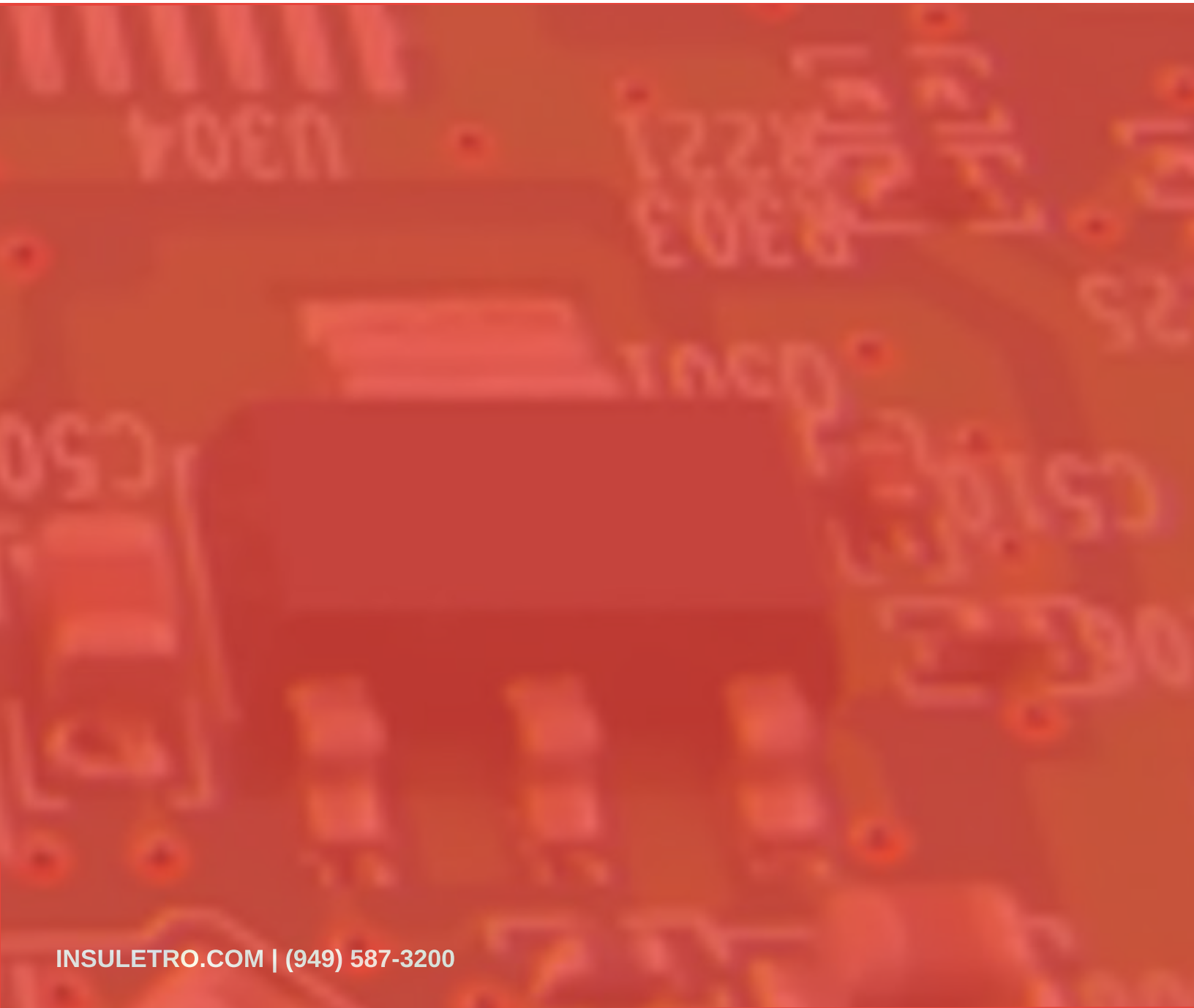


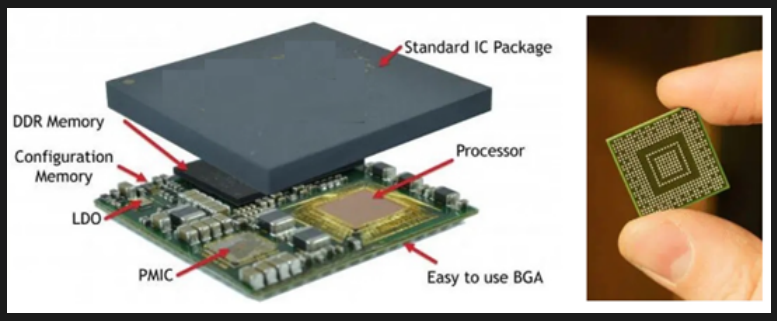
TABLE OF CONTENTS

ABSTRACT

One of the main benefits of microelectronics is the ability to create circuits with devices that are smaller, faster, and more energy efficient than traditional electronic devices. When technology advancements require these metrics to be improved, they challenge one another. The more gates used in an IC, increases the functionality and the power requirements, causing thermal challenges and size increases. The industry responds by lowering the voltage requirement and reducing the size of gates, cells, and interconnects, which now allows for an increase in all the metrics.

Integrated Circuit Scales of Integration based on Number of Internal Logic Gates	
Complexity	**Number of Gates (Components or cells)**
Small Scale Integration (SSI)	< 12
Medium Scale Integration (MSI)	12 to 99
Large Scale Integration (LSI)	100-9,999
Very Large Scale Integration (VLSI)	10,000 to 99,999
Ultra Large Scale Integration (ULSI)	100,000 to 999,999

The component type with the most terminals is the Ball Grid Array (BGA). BGAs typically have a silicon chip that may be mounted with wire-bonds or flip-chip. They are placed on an interposer PCB that has Z-axis routes to a standard pattern BGA terminal that mounts on a standard PCB. BGA's package size follows four main indexes: Overall package size, number of terminals on one device, terminal size, and the centerline pitch between terminals. These metrics range depending on functionality: Package size up to 0.6 to 100mm, number of terminals 4 to 10,000, terminal size .15 to 0.5mm, and terminal pitch of .25 to 1.0mm. As soon as this article goes to print someone one-ups these numbers.

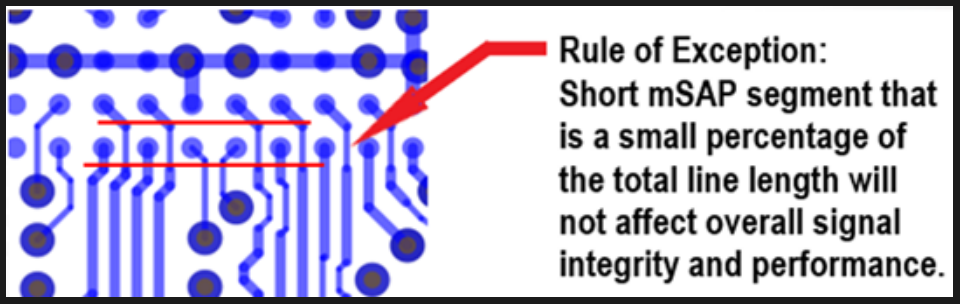


Dense System on a Chip Combined onto a BGA Package Substrate

BACKGROUND

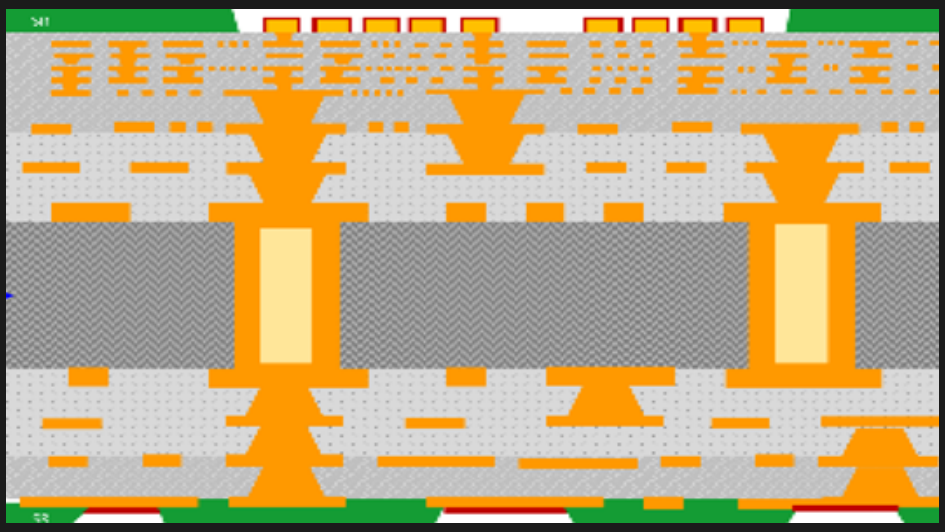
These dense fine pitch devices have been used for some time now in our industry and the demand will only increase. Although innovated mostly in the States, the majority (some 95%) are currently produced offshore and now the US Government Chips Act is an effort to bring the development of ICs, plus Package Design back to the States, and this is to be applauded. Intel and several other IC foundries are slated to come online in the US approximately in the next 3-5 years. The need for US PCB fabricators to be capable to build package design interposers is right alongside in this endeavor. Package Interposers have incredibly small Modified Semi Additive Process (mSAP) trace widths and are used with specialized laminates that are available in very thin dielectric thicknesses. These also use other 3-D interconnect solutions such as Ormet® sintering paste. This is also to be applauded as a welcome recapture of American innovation supported by American manufacturing.

At Insulectro we are the industry leading distributor of all PCB Fabrication Process supplies and materials for rigid and flex circuits. We have been pioneering how the entire industry should position themselves for supporting the next generation of Micron-Interconnect and Embedded Circuitry **within the standard PCB**. As we have looked into these topics, we have seen several misconceptions as this is viewed from a limited perspective. The immediate response is often to quote what you know about the smallest mSAP trace width you've heard of or that you've seen built. But what often gets omitted is the fact that the performance of a thin mSAP trace, **will not perform at 50 Ω with ample current carrying capacity for a full trace length using standard materials**. Currently mSAP is only used at a short length and the signal integrity problems are tolerated. This can be referred to as the "Exception Rule."



PCB Standards In The Future

The standard PCB of the very near future should prepare for Micron Interconnect that **performs at 50 Ω with ample current carrying capacity for a full trace length using standard materials w**ith today's available process aids and materials. Some Package Interposers will go away putting the need of the chip on the board. This will require some technology advancements. But you must understand what needs to be done, what materials and process aids will support this need. So many people are looking at this need with a singular perspective. This next generation solution must address the design solvability, the performance requirements, and the manufacturing requirements. Insulectro is currently working to test and verify specific design metrics and provide next generation laminate materials with process aides to build the PCB micron interconnect of the future..



Future Highbred Board will Merge Chip on Board, mSAP with Standard and Advanced PCB Materials plus Required Process Steps

CONCLUSION

Come and learn more about this interesting subject. As a fabricator, if you're interested in partnering in this research and development, please contact your Insulectro representative and let us help you and your fabricator build the board of the future now.

As we present our products and services to you and your company, we want you to know Insulectro's Design Education Program is eager to freely support signal-integrity reviews of design circuits prior to fabrication. Also, we are ready and eager to create one or several training sessions for the OEM or your fabrication team. These will be tailored to meet the exact needs of the audience, brought by a technically appropriate presenter, with specific content to further your team's success and provide that edge to meet the needs of advancing technology trends. Contact any of our Technical Account Managers or call any of our branch offices to schedule your **Virtual Training Session** soon.

Mike Creeden, Technical Director Design Education
Reminding you to make technically appropriate material decisions and to get the best use of the best material.