Advanced Via Solutions (Part 3/3)

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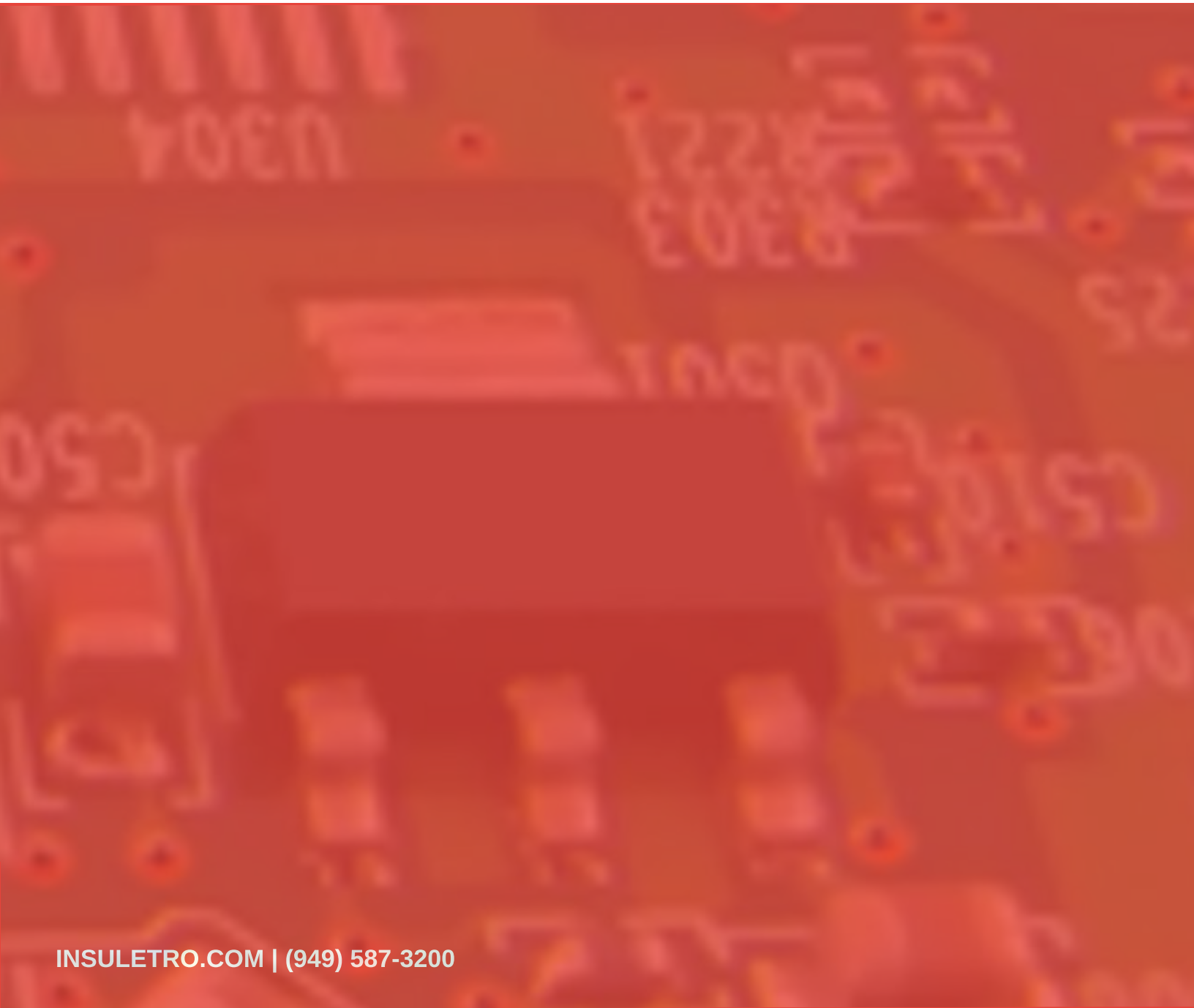

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ABSTRACT

Today's circuit boards often contain many rationales to implement HDI routing strategies.

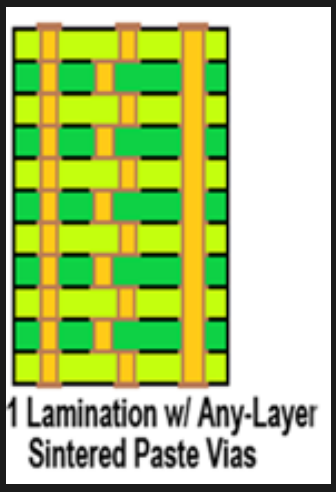
HDI/Microvia Routing – There are several reasons to consider using HDI technology when routing a circuit board. The most common of which is to improve the routability of the devices on the board, this means how many traces per each layer. To use HDI/microvias most efficiently, it is best to make HDI decisions early in the design process and to use the microvias all over the board. While drilled individually, the drilling is done so quickly that liberal use of them is encouraged. Once the technology is added to a board, there is no extra cost to using it all over the board. Also, considering the concept of a balanced construction, if you use them on one side of the board you will have the freedom to use them on the opposite side of the construction whether you use them or not.

HDI technology provides some benefits to the design's routing, as well. The microvias can increase the flexibility of the routing solutions available by setting up everything from simple to elaborate patterns of vias anywhere on the board. They allow for much more routing on any one layer because there are no thru holes to route around. Electrically, HDI can have better signal integrity because of stub elimination and reduced switching noise through smaller and shorter via structures. Also, they have better EMI control because of improved containment of energy fields since the signals are closer to their return planes with the use of thinner dielectrics.

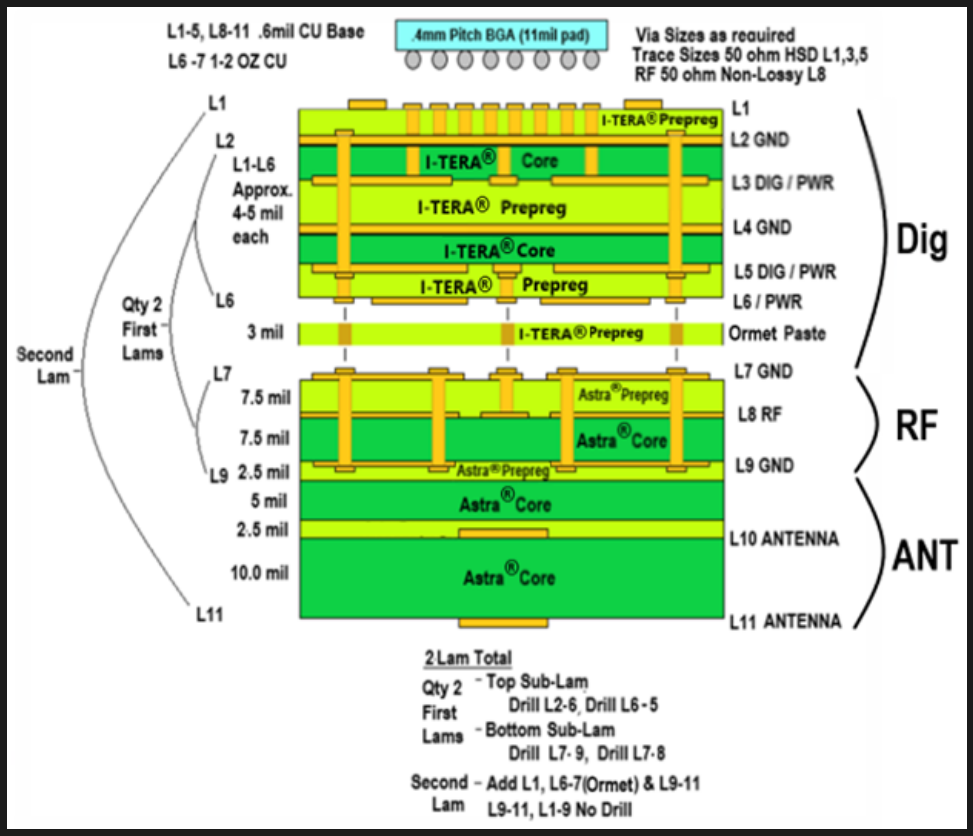
When deciding to use microvias, it is a good idea to plan for the signal routing. The designer will need to think about how all the complex buses will flow from one layer to another ahead of the actual routing. In planning routing fanout options, sketch out a via utilization strategy.

BACKGROUND

Ormet® Sintering Pastes Allows Any Layer Via Usage – This is often used when no restricted via usage is required. This is often utilized on BGA package designs with thin, high layer count interposer boards or Telecom 5G boards that have a hybrid circuitry combination of High Speed Digital (HSD), RF, and antenna circuitry all on one board. As shown below.

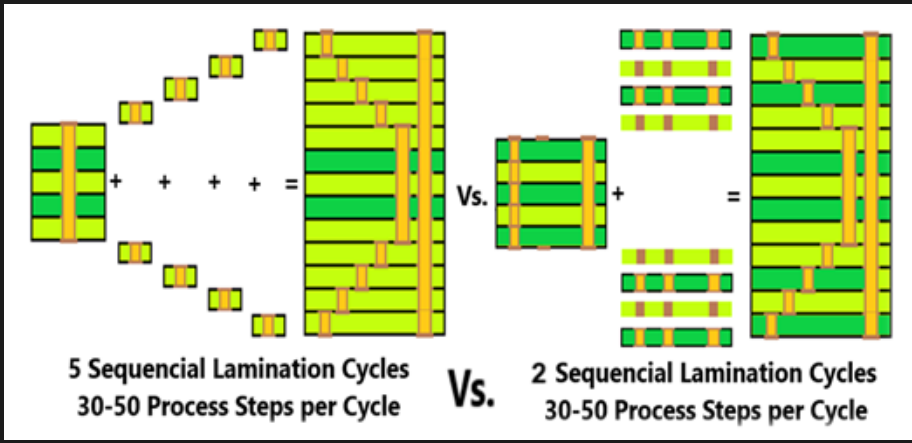


1 Lamination w/ Any-Layer Sintered Paste Vias



MULTI-LAMINATION BUILDS

Ormet® Sintering Pastes Solves Issues for Multi-lamination Builds - The most common method used today by designers in layout for HDI Boards often termed as a, "4N4," as shown in the left image below. The center core of layers referred to as the "N layers" is laminated, drilled, and plated, and then depending on the BGA pitch and pin count you might require 3 or 4 additional sequential lamination layers to pin escape with microvias. This must be repeated on the opposite side (as mentioned earlier) whether needed or not due to balanced fabrication construction processes to avoid warp and twist. This required multiple lamination process employs approximately 30-50 process steps per lamination cycle. This comes with a significant cost and time adder. These multiple process cycles stress the board decreasing long term reliability to the vias and the entire board bringing about intermittent via failures, due to all thermal excursions from manufacturing, environment, and circuit operation.



This 4N4 construction depicted on the left image above, may require 150-200 total process steps and 4-5 weeks on the calendar. Using the Ormet® Paste Z-Interconnects as an alternate solution, as shown in the right image below, can reduce this construction down to 2 cycles with 60-100 total process steps and about 2 weeks to fabricate.

Reduces Lamination Cycle Stress on material (Td) and via long term reliability.

CONCLUSION

These white papers have shown several cost saving technology solutions using the Ormet® Sintering Paste materials and process to several of the current challenges we are facing with HDI requirements. The request to implement these solutions using sintering paste must come from the OEM, as the fabricators job is to follow your innovation requests, and not ask you to follow their innovation. They need to be ready to deliver what you request and most of them are ready!

As we present our products and services to you and your company, we want you to know Insulectro's Design Education Program is eager to freely support signal-integrity reviews of design circuits prior to fabrication. Also, we are ready and eager to create one or several training sessions for the OEM or your fabrication team. These will be tailored to meet the exact needs of the audience, brought by a technically appropriate presenter, with specific content to further your team's success and provide that edge to meet the needs of advancing technology trends.

Contact any of our Technical Account Managers or call any of our branch offices to schedule your Virtual Training Session soon.