Advanced Via Solutions (Part 2/3)

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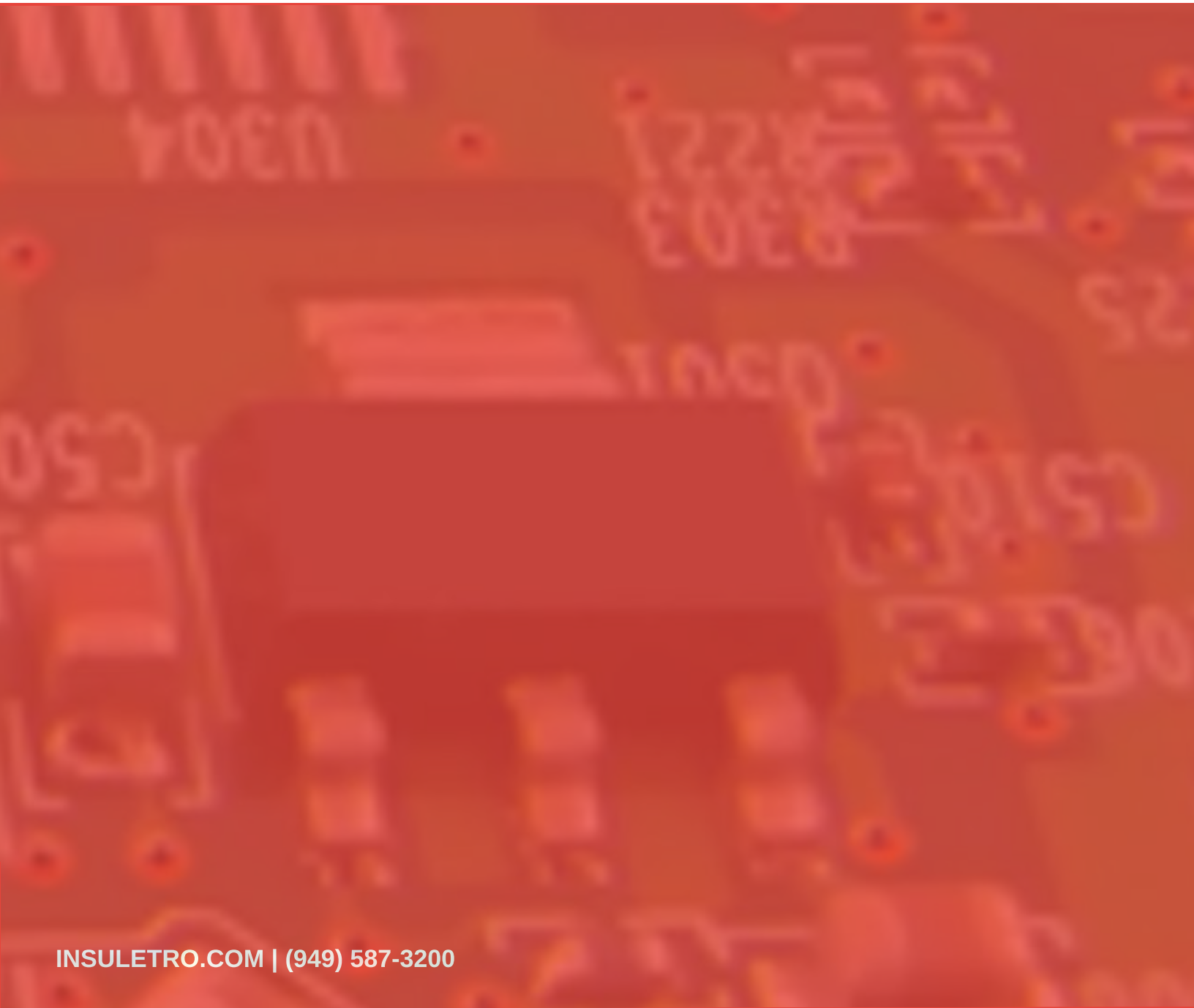

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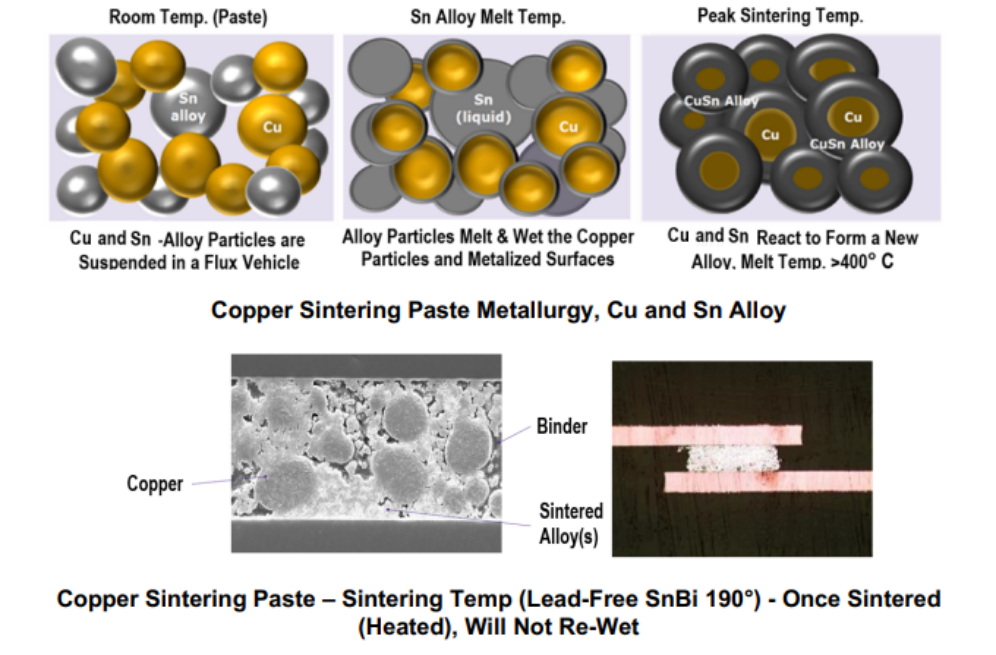
ABSTRACT

Advanced circuit requirements are presenting new challenges every year. These challenges are driven by the ever-increasing circuit needs to be smaller, faster, accomplish more, be cheaper, and often must be completed quicker. So, each year we try to meet these needs by working smarter, faster, more efficiently, adding technology and innovation. One of the most challenging features on our circuit boards are the vias by which we make Z-axis Interconnects. Advanced challenges require advanced innovations. We will continue to take a look at the challenges that vias are facing over these next two articles.

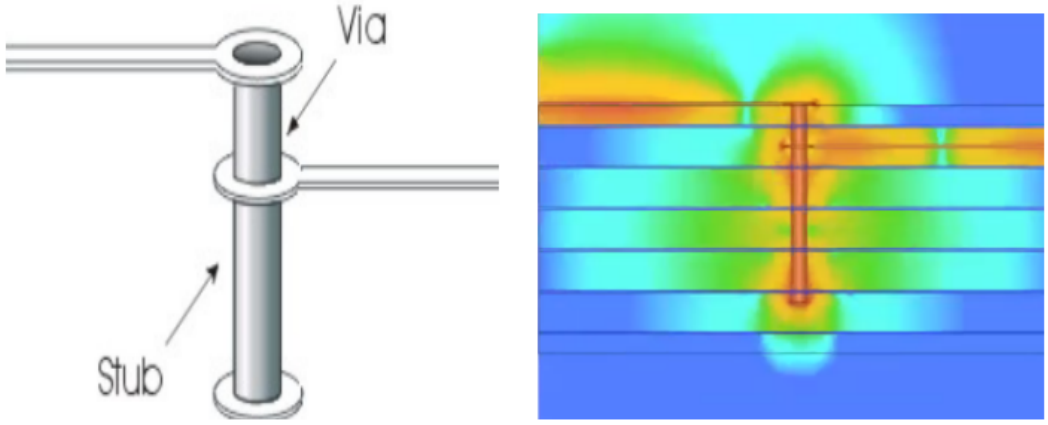


Z-axis Interconnects can be completed by a technology called, Transient Liquid Phase Sintering (TLPS) materials, which is the use of copper sintering paste, i.e., Ormet® Paste Z-Interconnects, this can be a very helpful alternative solution to conventional microvias. Ormet® Paste is an alloy compound of Copper (Cu), Tin (Sn), and Bismuth (Bi) used as the binding agent.

- TLPS is processed at temperatures well below the final usable temperature limits, forms alloys that does not re-melt under lead-free reflow conditions
- TLPS establishes metallurgical connections with copper interfaces, maximizes electrical and thermal transfer with solderable adherents
- TLPS creates Z-axis Interconnects during lamination, reduces lamination cycles

BACKGROUND

Ormet® Sintering Pastes have been utilized in industry for well over a decade. In fact, every reader of this article probably has these contained within the phone in your pocket or on almost every BGA interposer on your circuit boards. The current needs of everyday designs have now caught up to the advanced requirements used in telecom and BGA package designs with thin, high layer count interposer boards.

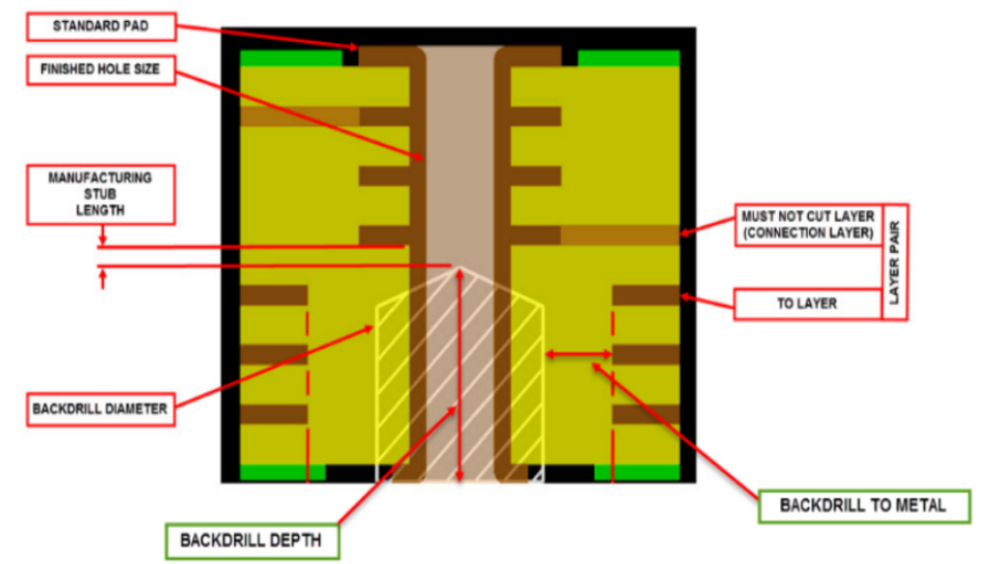


Radiating Via Stubs, Typically Unacceptable on a high Speed and RF Circuits

Today's circuit boards often contain extremely high-speed circuitry and the use of vias can cause unwanted radiating emissions from via stubs when a signal is routed on an inner layer but under a GND layer.

BACKDRILLING

Backdrilling is an alternate via type that may be utilized to confront this issue of parasitics from via stubs. Controlled Depth Drilling, a.k.a. Backdrilling, is removing the unused portions of a thru-hole via. Identify these with a slight change to the drill size and consider hole treatment to prohibit contaminants in the remaining hole. Depending on how many backdrill instances are required to solve a circuit, careful research should be made when considering alternate via types such as cost, reliability, and performance.

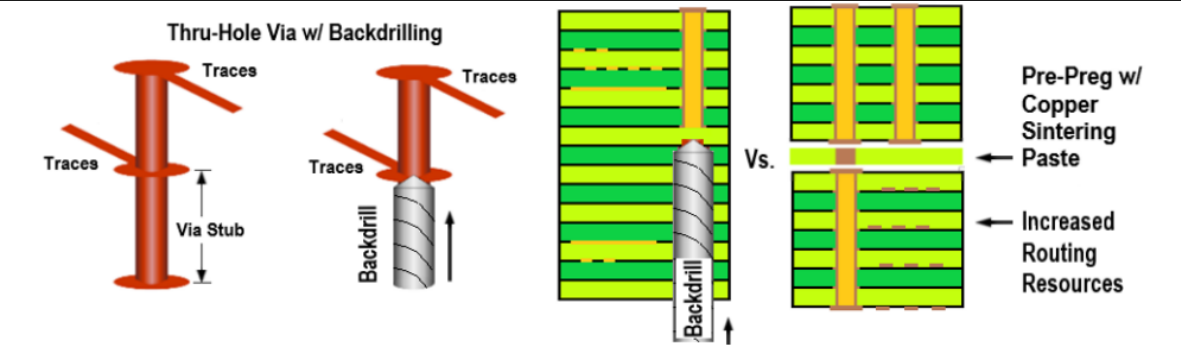


Backdrilling Clearances for Manufacturing Process Allowances

Backdrilling Clearances – Because backdrilling is a secondary fabrication process handled with some written instructions, it is imperative that design data provides adequate clearances in the X/Y & Z axis. It is recommended to assign a unique hole size that has a very slight difference for the purpose of identification and creation of a separate drill file. It is also recommended to allow the fabricator to remove unused pads on back-drill layers, because they may serve a temporary purpose for alignment, and you would not want copper pour to flood in around the smaller drill wall.

BACKDRILLING

Ormet® Sintering Pastes Eliminates Controlled-depth Backdrilling requirement for high-speed signals, thus eliminating parasitic stubs, adding routing resources prohibited by backdrilling, as shown in the image below.

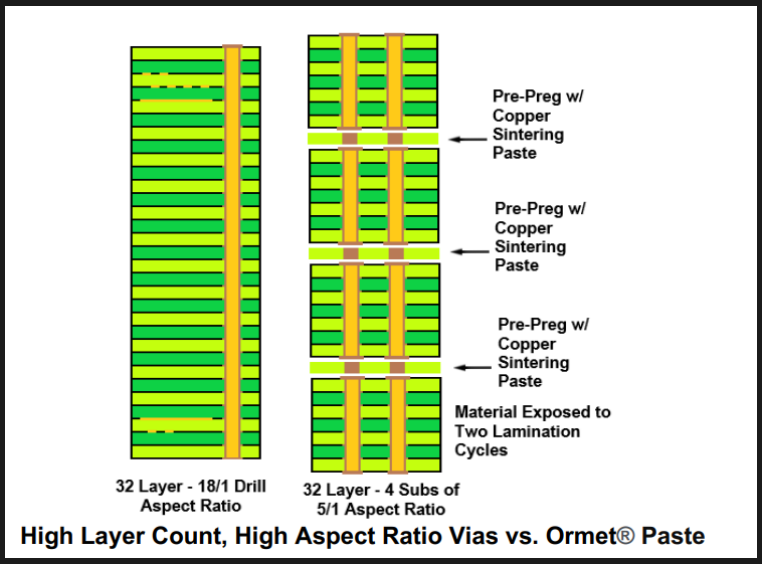


Backdrilling Used to Remove Via Stubs on High-speed Signals vs. Ormet® Paste

Ormet® Sintering Pastes Helps Solve High Layer Count Boards – There is a challenge that engineers face when circuits require a high number of layers to complete the routing using small thru vias. These circuits also have the requirements of using small conventional vias to pin-escape the µBGA's pin pitch.

These vias with a small pad and drill size create producibility challenges for fabricators due to the high aspect ratio of the via compared to the overall board thickness. This scenario creates a significant reliably issue with plating and drill break out. The usage of thru vias also significantly reduces the routing real estate on all layers of the board.

An unbuildable via hole aspect ratio board (as shown in the right image) often requires using a via with an 18:1 drill aspect ratio. Yes, this can be done but its costly and has low producibility. Using the Ormet® Sintering Paste materials and process to join several sub-composites together, completely resolves high aspect ratio plating problems.



High Layer Count, High Aspect Ratio Vias vs. Ormet® Paste

CONCLUSION

In our next Whitepaper, we will show a few more cost-saving, technology solutions to several of the current challenges we are facing. The request to implement these solutions using sintering paste must come from the OEM, as the fabricator's job is to follow your innovation requests, and not ask you to follow their innovation. They need to be ready to deliver what you request and most of them are ready!

As we present our products and services to you and your company, we want you to know Insulectro's Design Education Program is eager to freely support signal-integrity reviews of design circuits prior to fabrication. Also, we are ready and eager to create one or several training sessions for the OEM or your fabrication team. These will be tailored to meet the exact needs of the audience, brought by a technically appropriate presenter, with specific content to further your team's success and provide that edge to meet the needs of advancing technology trends.

Contact any of our Technical Account Managers or call any of our branch offices to schedule your Virtual Training Session soon.