Advanced Via Solutions (Part 1/3)

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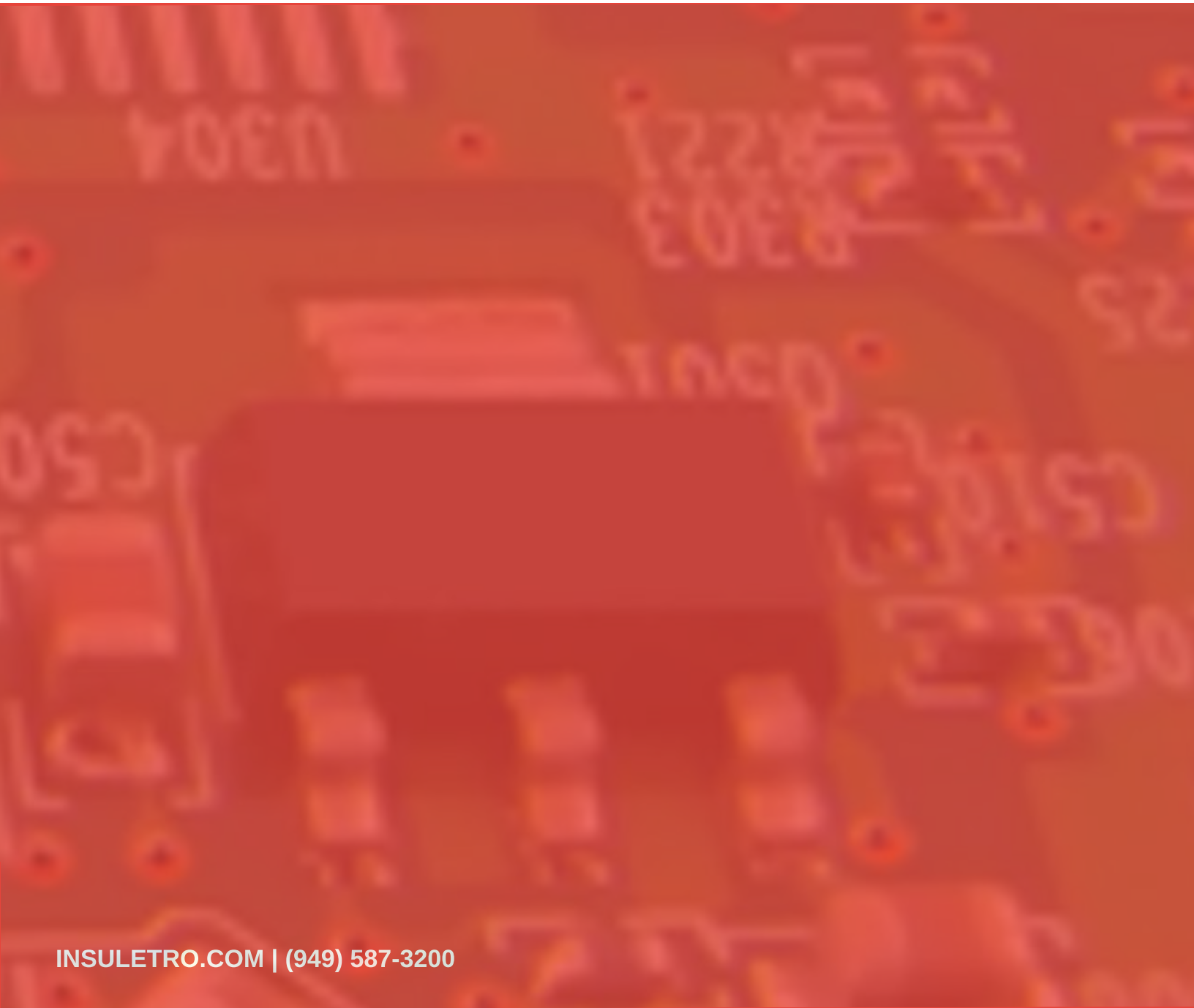
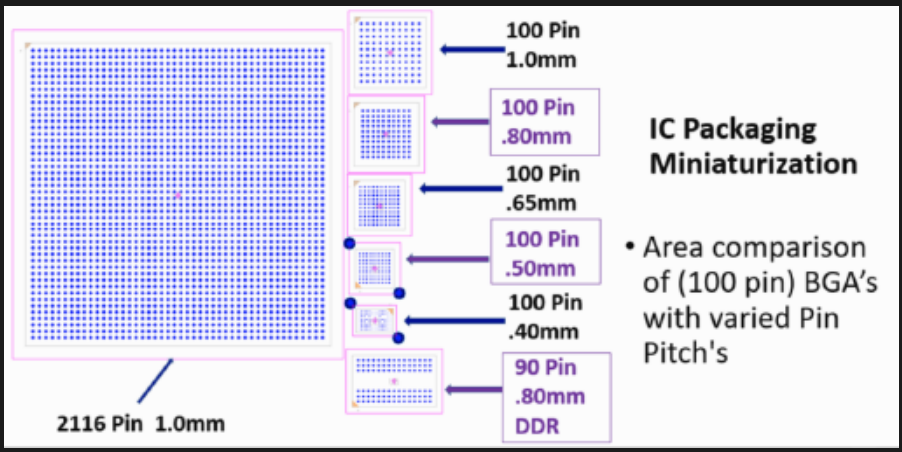


TABLE OF CONTENTS

ABSTRACT

Advanced circuit requirements are presenting new challenges every year. These challenges are driven by the ever increasing need to be smaller, faster, accomplish more, be cheaper, and often must be accomplished quicker. So, each year we try to meet these needs by working smarter, faster, more efficiently, adding technology and innovation. One of the most challenging features on our circuit boards are the vias by which we make Z interconnects. Advanced challenges require advanced innovations. We will take a look at the challenges that vias are facing over the next three articles.

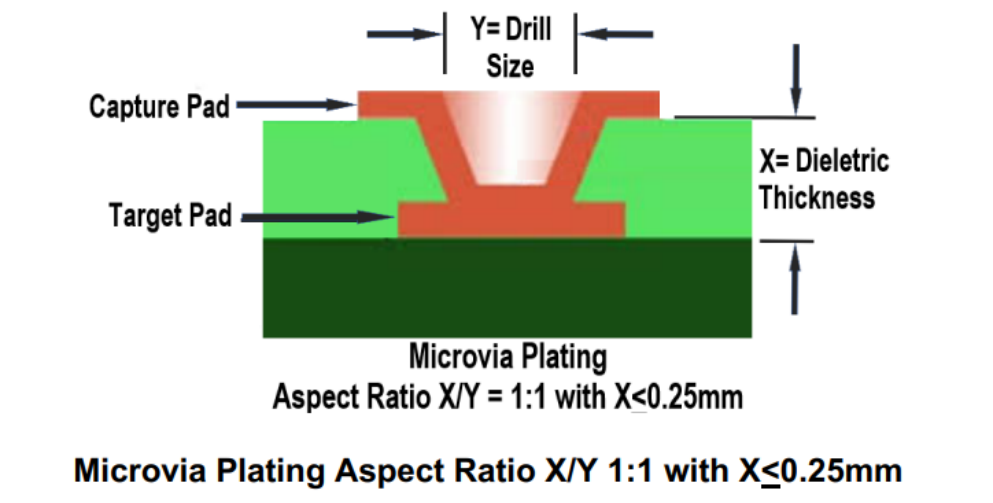
The historical overview on conventional vias is as follows: Z-axis Interconnects are used to continue a signal from one layer to another. They are typically drilled, treated, plated with copper, and then filled. There are many relational features that make for what is known as a Producibility Level indicating potential for high yield, low cost, and reliability.



High Density Interconnect (HDI) has been driven in the industry by the need to put more functionality into the ICs on our boards. More functionality in our devices is typically the adding of more transistors in the silicon enabling more and faster operations. More transistors creates more heat, so the voltage is always being lowered. This causes the transistors to be reduced in size on the silicon and then the number of pins on BGA chips increases, yet the actual package size gets smaller. This is accomplished by reducing the land pad size along with the pin pitch of separation in the grid array. The image below shows several 100 pin BGA packages with reduced pin pitches.

BACKGROUND

Many engineers when confronted with the potential to utilize HDI respond with, “We don’t like to use HDI”. What that inexperience really conveys is that they do not comprehend the fact that HDI is no longer a choice once they have selected to utilize BGAs with a .65mm pin pitch or smaller. HDI becomes a requirement and not a choice, in most instances. Microvias are used extensively with HDI µBGAs .65mm and below. A microvia is often laser drilled with a .75:1 aspect ratio drill depth to width. They are plated, filled, coplanar finished and should not be stacked upon other drills for reliability reasons.



Microvia Plating Aspect Ratio X/Y 1:1 with X≤0.25mm

Per IPC-2221 Section 1.5 1 - A microvia is defined as a blind structure (as plated) with a maximum aspect ratio of 1:1 when measured in accordance with Figure 1-1, terminating on or penetrating a target pad with a total length of no more than 0.25 mm [0.00984 in] measured from the structure’s capture pad to the target pad.

MICROVIAS

Microvias have been utilized in the industry for a long time and significant empirical analysis has shown that with the current physical parameters and the current manufacturing processes there have been significant reliability concerns. With any method or material used when connecting microvias layer to layer, it is always highly recommended to practice staggering vias when transitioning layer to layer and never stack microvias on top of another as they can lower the producibility and lower the reliability due to the difference in the Z-axis Interconnects expansion of the laminate material as compared to a metal via structure. And never place a microvia over a thru via structure.

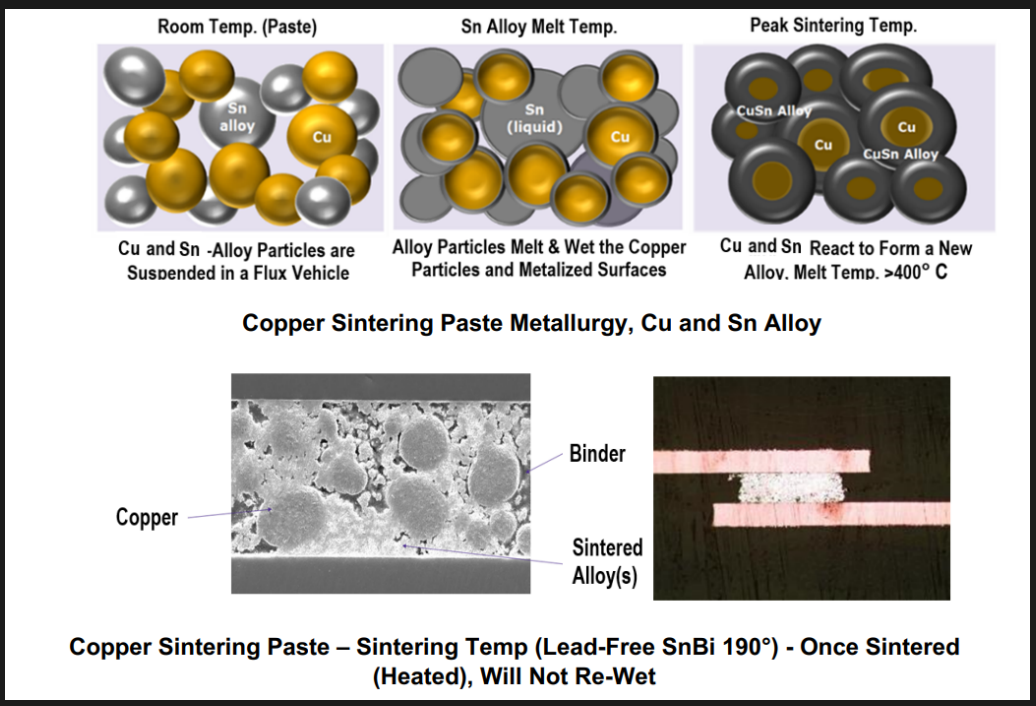
Always Stagger, Never Stack Microvias – Never Stack Microvia Over Thru Hole

With the need for microvias not going away, coupled with the reliability concerns of conventional plated microvias, it is time to look at an exciting alternative to Z-axis Interconnects called, Transient Liquid Phase Sintering (TLPS) materials, which is the use of copper sintering paste, i.e., Ormet® Paste which can be a very helpful alternative solution. Ormet® Paste is an alloy compound of Copper (Cu), Tin (Sn), and Bismuth (Bi) which is used as the binder.

- TLPS is processed at temperatures well below the final usable temperature limits, forms as an alloy that does not re-melt under lead-free reflow conditions
- TLPS establishes metallurgical connections with copper interfaces, maximizes electrical and thermal transfer with solderable adherents
- TLPS creates Z-axis Interconnects during lamination and reduces lamination cycles

CONCLUSION

Ormet® Sintering Pastes have been utilized in industry for well over a decade. In fact, every reader of this article probably has these contained within the phone in your pocket or on almost every BGA interposer on your circuit boards. The current needs of everyday designs have now caught up to the advanced requirements used in telecom and BGA package designs with thin, high layer count interposer boards. Our PUMANEWS™ NEWSLETTER will show several cost saving, technology solutions to several of the current via challenges we are facing by using the Ormet® Paste Z-Interconnects materials and processes to solve HDI requirements.



As we present our products and services to you and your company, we want you to know Insulectro's Design Education Program is eager to freely support signal-integrity reviews of design circuits prior to fabrication. Also, we are ready and eager to create one or several training sessions for the OEM or your fabrication team. These will be tailored to meet the exact needs of the audience, brought by a technically appropriate presenter, with specific content to further your team's success and provide that edge to meet the needs of advancing technology trends.