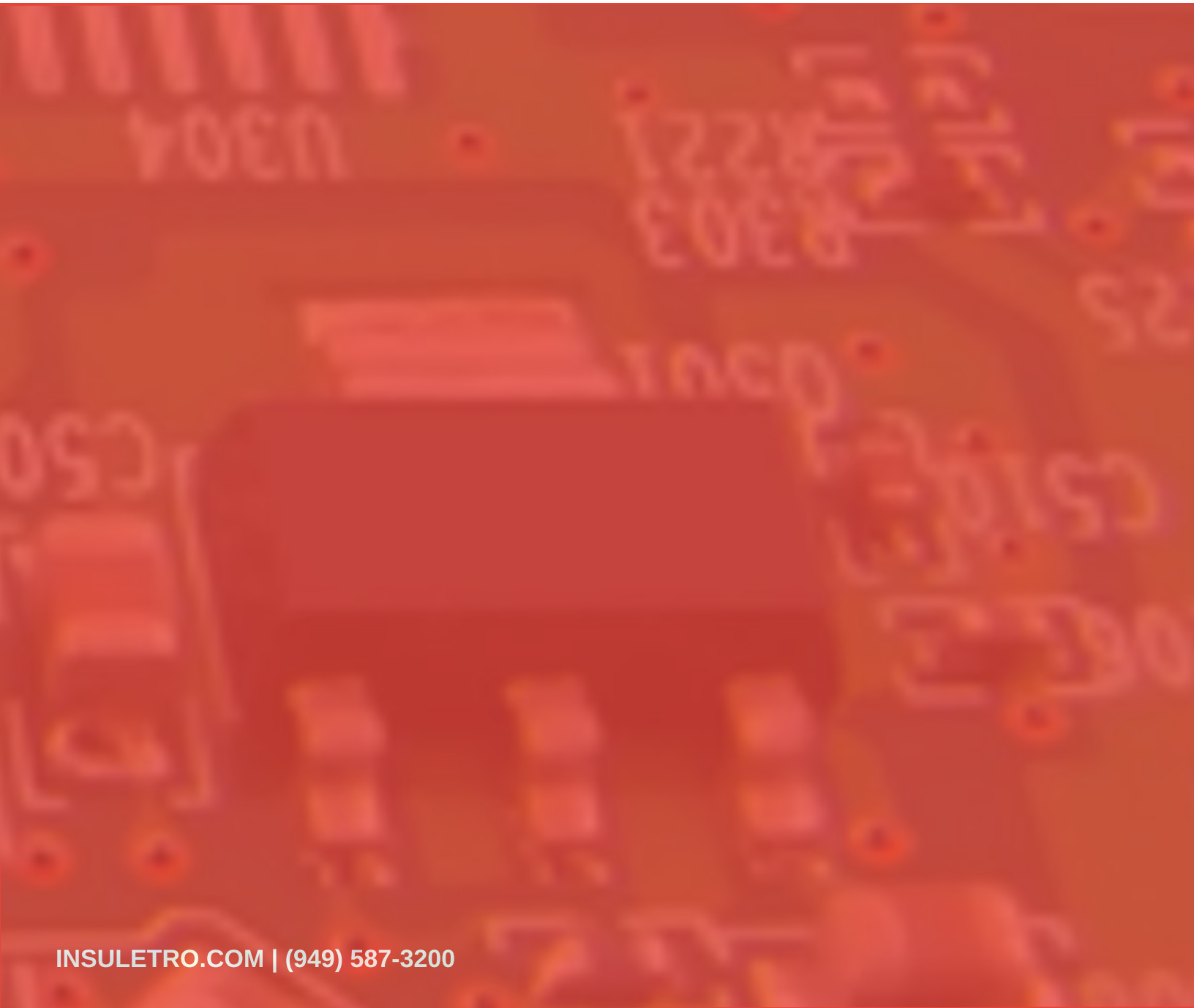
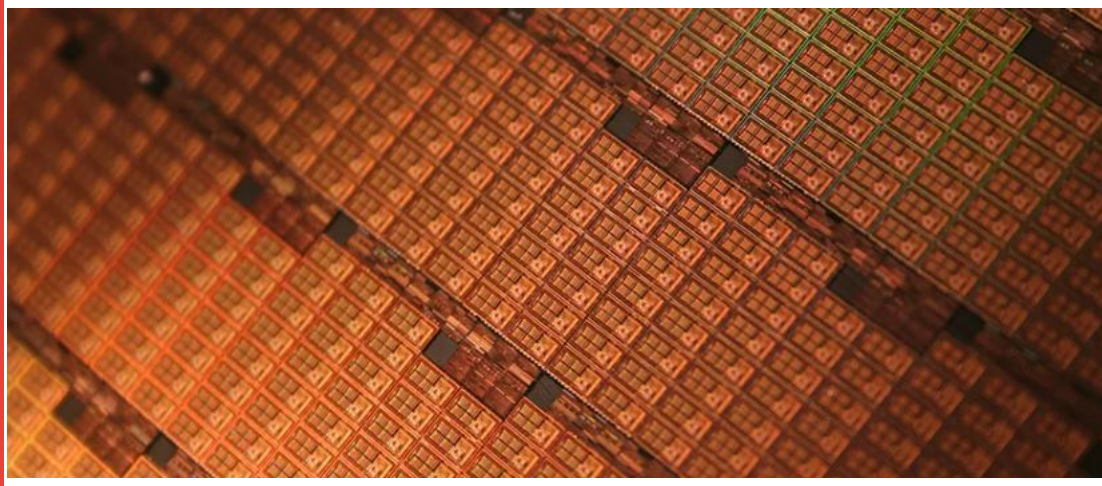
INSULECTRO

Copper Electroplating Fundamentals



TABLES OF CONTENTS



OVERVIEW

Evolution of Bumping

Copper pillars are now common in flip chip interconnection, usually with a lead-free SnAg solder cap on top. The transition to copper pillars has been driven by the limitations related to size and pitch (space between features) of traditional controlled collapse chip connection (C4) bumping. As pitch requirements continue to shrink, copper pillars can enable higher-density designs while maintaining sufficient bump height. The next-generation technology will feature pillars as narrow as 10 to 30 µm.

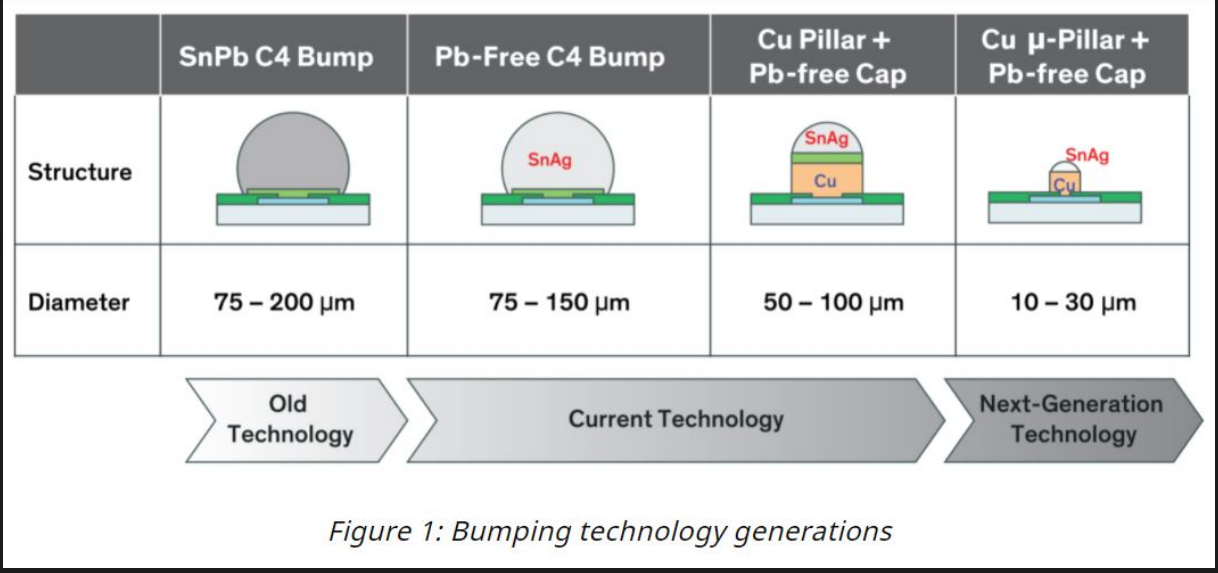


Figure 1: Bumping technology generations

Copper Pillar Plating Process

Capped Copper Pillar Platting Process

Copper pillars are electroplated over a Cu seed layer at the base, with photoresist defining the diameter of the pillar. A nickel diffusion barrier between the pillar and the solder cap limits formation of a copper-tin intermetallic layer at the interface or prevents formation of microvoids. Excessive intermetallic growth and microvoids can both negatively affect reliability. When used with copper chemistry that has exceptionally high purity, this nickel barrier may or may not be needed, depending on customer preferences.

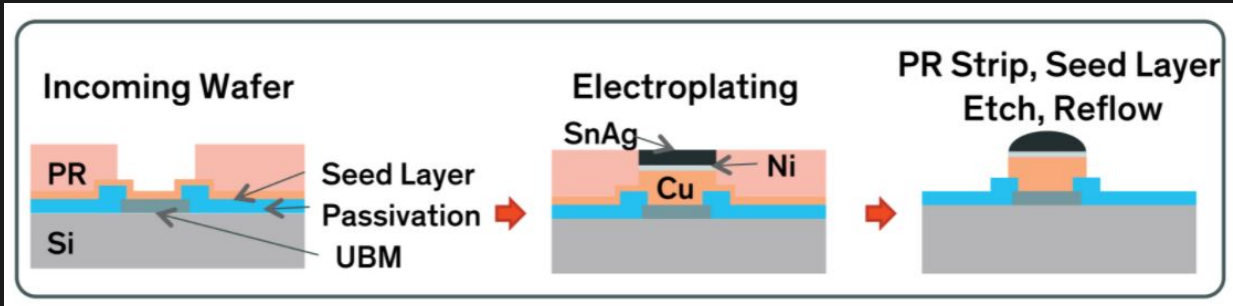


Figure 2: Illustration of the tin-silver capped copper pillar plating process

Design and Performance

Proper choice of electroplating materials and processes ensures that pillars meet certain design goals, chosen to optimize quality and reliability. Keeping the impurity level in the plating bath as low as possible minimizes the risk of developing voids at the pillar-solder interface. If dopants such as carbon, sulfur, chlorine and other impurities are kept below 20 ppm, it is possible to form a void-free capped pillar even without using a nickel barrier layer.

Design Goal	RDL Target	20 µm Pillar Target	RDL Target	50 µm Pillar Target
%WID Uniformity	<5%	<5%	<5%	<5%
Plating current desties	2 to 12 ASD	4.5 to 12 ASD	4.5 to 18 ASD	20 to 40 ASD
Total Doping (C,N,O,S,CI)	<20 ppm	<20 ppm	<20 ppm	<20 ppm
Solder Compatibility	Void-free w/o Ni Barrier	Void-free w/o Ni Barrier	Void-free w/o Ni Barrier	Void-free w/o Ni Barrier

Effects of Electrochemical Potential

Pillar height needs to be consistent for proper die attach, but electrochemical potential is not uniform across each die on a wafer. It will be higher at the edges and corners, resulting in taller bumps at the edge and therefore insufficient contact at the center of the die, where the pillars are lower. The higher the bump density, the greater the challenge.